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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/079,472	02/19/2002	Maitreyee Mahajani	40025-005	6706
33971	7590	12/09/2004	EXAMINER	
MATRIX SEMICONDUCTOR, INC. 3230 SCOTT BOULEVARD SANTA CLARA, CA 95054			LE, THAO X	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 12/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/079,472	Applicant(s) MAHAJANI ET AL.	
	Examiner Thao X Le	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 November 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 3,5-9,23-26,28,29,32,33,36-38 and 40-42 is/are pending in the application.
- 4a) Of the above claim(s) 3,5-8,23,25,28,29,32,33 and 40-42 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 9,12-15,24,26 and 36-38 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of species of Fig. 1 in the reply filed on 19 Nov. 2004 is acknowledged. The traversal is on the ground(s) that claims 2, 23, 25, and 40-42 are generic to both identified species. This is not found persuasive because these claims are only generic to the identified species in fig. 2a and 2b, while claims 9, 24, 26, and 36-38 are generic to the identified species in fig. 1. The following Office action considers species of fig. 1 that has readable claims 9, 24, 26, and 36-38 and their dependent claims.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

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3. Claims 9, 12-15, 24, 26, 36-37 and 38 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6674138 to Halliyal et al.

Regarding to claims 9, 24 Halliyal discloses a method for making a SONOS device, comprising: providing a channel region 18, column 9 line 1, and providing a first oxide layer 28 on the channel region by ISSG process, column 10 line 33, providing a nitride layer 30, on the first oxide layer 28, and providing a second oxide layer 32, column 8 line 63, on the nitride layer 30, wherein the device is a SONOS.

With respect to nitride layer 30, Halliyal discloses structure 26 is a modified ONO (28/30/32) structure, column 8 line 27, that can be a combination of various materials including high k material is added to the nitride layer 30 of the conventional ONO, column 12 lines 15-20. Thus Halliyal either inherently or implicitly discloses nitride layer

Regarding claims 12-15, Halliyal discloses a method wherein the ISSG is performed at a temperature ranging from 700°C to about 1150°C, column 11 line 17, wherein the pressure ranging from 100 torr to about 300 torr, column 11 line 9, wherein the ISSG oxide layer 28 having the thickness of 10 to about 150 angstrom, column 11 line 65, wherein the transistor is a SONOS transistor, wherein the method further including annealing the oxide layer 18 in a nitric oxide atmosphere, column 7 line 39.

Regarding claim 26, Halliyal discloses an integrated circuit containing a SONOS semiconductor device made by the method comprising: providing silicon 16, column 10 line 3, providing a first oxide layer 28 on the silicon layer 16 by ISSG, column 10 line 33, providing a nitride layer on 30 on first oxide layer, and providing a second oxide layer 32, column 8 line 63, wherein the device is a SONOS device, wherein the gate 24 comprises metal, column 15 line 40.

With respect to nitride layer 30, Halliyal discloses structure 26 is a modified ONO (28/30/32) structure, column 8 line 27, that can be a combination of various materials including high k material is added to the nitride layer 30 of the conventional ONO, column 12 lines 15-20. Thus Halliyal either inherently or implicitly discloses nitride layer 30. Regarding claims 36, 37, Halliyal discloses a method for making a SONOS device, comprising: providing a channel region 18, providing a first oxide layer 28 in contact with the channel region by an in-situ steam generation process, column 10 line 33, providing a nitride layer 30 in contact with the first oxide layer; and providing a second oxide layer 32, column 8 line 63 in contact with the nitride layer, fig. 1.

With respect to nitride layer 30, Halliyal discloses structure 26 is a modified ONO (28/30/32) structure, column 8 line 27, that can be a combination of various materials including high k material is added to the nitride layer 30 of the conventional ONO, column 12 lines 15-20. Thus Halliyal either inherently or implicitly discloses nitride layer 30. Regarding claim 38, Halliyal discloses an integrated circuit containing a SONOS semiconductor device made by a method comprising: providing a silicon wafer or silicon layer 16, fig. 1, providing a first oxide layer 28 in contact with the silicon wafer or silicon layer 16 by an in-situ steam generation process, column 10 line 33, providing a nitride layer 30 in contact with the first oxide layer; and providing a second oxide layer 32 in contact with the nitride layers, fig. 1, wherein the device is a SONOS semiconductor device.

With respect to nitride layer 30, Halliyal discloses structure 26 is a modified ONO (28/30/32) structure, column 8 line 27, that can be a combination of various materials

including high k material is added to the nitride layer 30 of the conventional ONO, column 12 lines 15-20. Thus Halliyal either inherently or implicitly discloses nitride layer

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
06 Dec. 2004



HOAI PHAM
PRIMARY EXAMINER